

REMARKS

The Examiner's Office Action of May 6, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By this Amendment, claims 1, 3, 6, 9, 32, 33 and 34 have been amended. Accordingly, claims 1-45 are pending for consideration, of which claims 1, 3, 6, 9 and 32-34 are independent.

Referring now to the detailed Office Action, claims 1-9 are rejected under 35 U.S.C. 102(b) as being unpatentable over Applicants' admitted prior art in view of U.S. Patent No. 4,090,219 to Ernstoff et al. (hereinafter "Ernstoff") and U.S. Patent No. 4,750,813 to Ohwada et al. (hereinafter "Ohwada"). Claims 10-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Ernstoff and Ohwada as applied to claims 3 and 9 above, and further in view of U.S. Patent No. 5,528,262 to McDowall et al. (hereinafter "McDowall"). Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Ernstoff, Ohwada, and U.S. Patent No. 5,327,229 to Konno et al. (hereinafter "Konno"). Claims 35-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Ernstoff and Ohwada and Konno as applied to claims 32-34 above, and further in view of McDowall. In view of the amendments provided above and the comments to follow, Applicants respectfully traverse these rejections.

Initially, claims 1, 3, 6, 9 and 32-34 have been amended to include a feature variously setting forth that the thin film transistor(s) has(have) "a channel region comprising crystallized silicon." This feature is supported, for example, by lines 13-19 of page 28 in the specification. On the other hand, Applicants respectfully submit that Applicants' admitted prior art, Ernstoff and Ohwada do not disclose or suggest this feature.

Specifically Ohwada, previously cited as disclosing the claimed thin film transistor, does not disclose or suggest that the thin film transistors include "a channel region comprising crystallized silicon." After a review of the rejection and the Ohwada patent, Applicants can find no disclosure that the thin film transistors include "a channel region

comprising crystallized silicon”, as recited in each of the independent claims. While the Ohwada patent does appear to disclose a display portion 1 that comprises a transistor circuit consisting of TFT elements (see column 2, lines 41-49 of Ohwada), there is no specific disclosure regarding the makeup of the thin film transistors. In fact, there is no detailed discussion of TFT’s other than circuit diagram representations depicted in FIGs. 1, 2 and 10-12.

Moreover, in the Response to Arguments Section (page 8) of the Office Action, the Examiner appears to indicate that “...though Ohwada doesn’t specifically teach an n-speed field sequential color generation circuit being formed to a thin film transistor on the glass substrate, the teaching of the other circuitry, mainly the timing generation circuit is taught to be formed with thin film transistors...” and that “it would have been obvious to one having ordinary skill at the time of the invention to allow the n-speed sequential color generation circuit to be represented in the teachings of Ohwada by the timing generation circuit...”

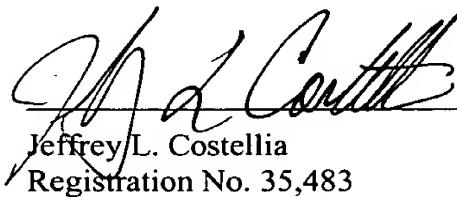
Applicants strenuously disagree with this line of reasoning provided in the Office Action. Applicants note that to establish a prima facie case of obviousness, (1) there must be some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art references when combined must teach or suggest all claim limitations. See MPEP § 2142-2143.

The examiner has provided **no explanation** as to why one skilled in the art, noting the Ohwada reference, which does not show said n-speed field sequential color signal generation circuit, would be motivated to employ thin film transistors over said substrate as also variously recited in the claims. Just because other elements in the Ohwada reference have thin film transistors, does not necessarily *allow* other elements to comprise thin film transistors, without some motivation to do so. Also, the Examiner has neither taken Official Notice or provided a prior art reference showing the missing feature. As discussed previously with reference to Ohwada, the Examiner is attempting to provide a general teaching directed to the n-speed field sequential color signal generator, which is recited in the independent claims of the present invention. Specifically, the “[m]ere fact that the prior art may be modified to produce the claimed invention does not make modification obvious unless prior art suggested the desirability of modification.” *In re Fritch*, 23 U.S.P.Q.2d 1780

(Fed.Cir.1992). The examiner cannot merely say that any variation from what Ohwada shows is "obvious" without showing some motivation to do so. In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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